National University of Computer and Emerging 

sciences

**Objectives:**

• To learn and understand how to design a multiple output combinational circuit using XOR and XNOR

• To learn and understand the working of different types of decoders

• To learn and understand how to design a multiple output combinational circuit using Decoders

**Exclusive-OR & Exclusive-NOR gates:**

The figure given below shows the symbol of Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates.



XNOR gate XOR gate

Boolean expression of XNOR gate is���� + ��̅��̅and Boolean expression of XOR is��̅�� + ����̅ . Boolean expression of XNOR gate can be implemented using XOR gate as shown in figure below:



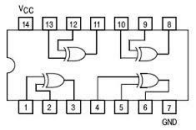
**Function Table:**

| **Inputs** | | **Output** |
| --- | --- | --- |
| **A** | **B** | **Y** |
| L | L | L |
| L | H | H |

| H | L | H |
| --- | --- | --- |
| H | H | L |

H= Logic High, L= Logic Low

**Connection Diagram:**

**74LS86 IC** will be used for implementation of XOR gate function. **74LS86 IC** contains four 2- input XOR gates. The function table and connection diagram for this IC are shown below: 

**2-to-4 line decoders:**

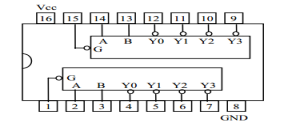
74LS139 IC contains two fully independent 2-to-4 line decoders with active low enables. The function table and connection diagram for this IC are shown below:

**Function Table:**

| **Enable** | **Selection**  **Inputs** | | **Outputs** | | | |
| --- | --- | --- | --- | --- | --- | --- |
| **G** | **B** | **A** | **Y0** | **Y1** | **Y2** | **Y3** |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

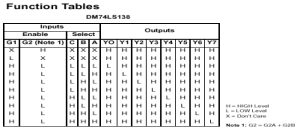
H= Logic High, L= Logic Low, X= Don’t Care

**Connection Diagram:**

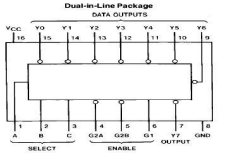
****

**3-to-8 line decoders:**

74LS138 IC contains 3-to-8 line decoder. The function table and connection diagram for this IC are shown below:



**Connection Diagram:**

****

**Lab Tasks:**

**Question 1:**

**Implement 2-4 Decoder using basic gates on Logic Works and with Decoder IC on Logic Trainer.**

i1 i0 d3 d2 d1 d0

0 0 0 0 0 1

0 1 0 0 1 0

1 0 0 1 0 0

1 1 1 0 0 0

**Question 2:**

Implement 3x8 decoder using two 2x4 decoders and not gate [Use Decoder IC ; Implement on L.W and L.T]

**Question 3:**

**4 bit parity Checker**

**1) implement a parity checker using decoder and OR gates**

A circuit that receives 4-bit message and outputs Error (E=0) if its parity is ODD **2) Implement it using XOR and XNOR gates**